

	2025		1		DISU434		01
							3-0-3
	EECE274() ,EECE273()						
	(11:00 12:15) -						
E-Mail	SHKANG@POSTECH.AC.KR			Homepage	SOC.POSTECH.AC.KR		
					054-279-2379		
Office Hours	TBD						
Understanding, designing, and optimizing digital circuits with respect to different quality metrics: speed (performance), power dissipation, cost (area) and reliability.# "Design a system yourself"							
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Attendance/Quiz (10) + Assignment (20) + MidTerm (20) + Final Exam (25) + Term Project (25)							
							ISBN
Weste/Harris, CMOS VLSI Design: a circuits and systems perspective (4th/E)							
Flipped Learning # # - Q&A lecture: Mon 11:00-12:15pm (Zoom)#							

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- Supplementary lecture: Wed 11:00 12:15 (Zoom, not every week)#

Zoom Link:#
<https://postech-ac-kr.zoom.us/j/85039383375?pwd=eIpHUGczVS9GMjVPRnZFZXJzdGFxQT09#>

ID: 850 3938 3375#
: 364231

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* 2/19() 11 Zoom . Zoom